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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): YOR9-2000-0844US (8728-479)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed name _____

Application Number	Filed
09/846,893	April 30, 2001

First Named Inventor: Erik R. Altman

Art Unit	Examiner
2183	Huisman, David J.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 48,909
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

_____
Signature

Nathaniel T. Wallace
Typed or printed name

516-692-8888
Telephone number

November 8, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Altman et al.	DOCKET: YOR920000844US1 (8728-473)
SERIAL NO.:	09/845,693	GROUP ART UNIT: 2183
FILED:	April 30, 2001	EXAMINER: Huisman, David J.
FOR:	**SYSTEM AND METHOD INCLUDING DISTRIBUTED INSTRUCTION BUFFERS HOLDING A SECOND INSTRUCTION FORM**	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Examiner:

In response to the Advisory Action dated November 2, 2006, Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal and a Pre-Appeal Brief Request For Review Form (PTO/SB/33).

REMARKS

Please consider the following reasons for this Pre-Appeal Brief Request For Review.

Claims 1-3, 5-13, and 15-21 are pending and stand rejected in the above-referenced application. Claims 1, 11, and 21 are the pending independent claims. Only objections and rejections pertinent to Claims 1, 11, and 21 are addressed here.

Claims 1-11, 13 and 15-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lavi et al. (USPN 6,453,407) in view of Ito et al. (USPN 5,742,782). The Examiner stated essentially that the combined teachings of Lavi and Ito teach or suggest all the limitations of Claims 1-11, 13 and 15-20.

Referring to Claim 1; the Examiner has indicated that "first and second instruction sets are broadly interpreted as first and second sets of instructions. Any group of instructions may be considered a set of instructions." Such an interpretation is contrary to the plain meaning of "instruction set" used in the art and as defined in the specification. For example, consider the dictionary definition of "instruction set" given as "the repertoire of arithmetic and logical operations of a computer. All programs exist in a computer as sequences of instructions drawn from the instruction set" (see Penguin Dictionary of Electronics, 3rd Ed. 1998). Indeed, the dictionary definition cited by the Examiner in the Advisory Action makes this distinction – that is an "'instruction set' as the set of machine instructions that a processor recognizes and can execute" (emphasis added). The definition does not state that any set is an instruction set, but rather that the set of machine instructions that a processor recognizes and can execute – that is all instructions a processor recognizes and can execute. Thus, an "instruction set" is not merely a group of instructions, but a repertoire of instructions available. Given the plain meaning of "instruction set," consider the following:

Lavi teaches a CLIW reference instruction is a decoded VLIW instruction word (see col. 9, lines 57-61). Lavi does not teach "providing a program of instructions comprising a plurality of instructions of the first instruction set and a plurality of instructions of the second instruction set, wherein the plurality of instructions of the first instruction set are decoded by a decoder in an execution pipeline and the plurality of instructions of the second instruction set are predecoded by a compiler" as claimed in Claim 1. Lavi teaches a single instruction set stored as decoded and undecoded instructions. Decoded and undecoded instructions of the same instruction set are not analogous to a first instruction set and a second instruction set, essentially as claimed in Claim 1. For example, Lavi's single instruction set is stored as both regular instructions and CLIW-reference instructions (see col. 16, lines 9-12); Lavi does not teach or suggest instructions and decoded instructions are from different instruction sets. Thus, Lavi fails to teach or suggest all the limitations of Claim 1.

Ito teaches that a decoder includes an instruction buffer (see Figure 3). Ito teaches decoding a single instruction set. Therefore, Ito fails to cure the deficiencies of Lavi.

Referring to Claim 11; Lavi teaches a CLIW reference instruction is discriminated from a regular instruction by an instruction decoder (see col. 10, lines 1-13). Lavi does not teach "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in Claim 11. Clearly, Lavi does not teach or suggest an execution queue (see for example, Figure 3). Indeed, Lavi teaches that instruction decoders operate in parallel with the CLIW array to further analyze all additional information stored in the reference instruction (see col. 10, lines 13-17). The instruction decoders and CLIW

operate in parallel on the reference instruction. Thus, Lavi fails to teach or suggest de-gating a plurality of execution queues storing the plurality of instructions of the first instruction form. Accordingly, Lavi fails to teach or suggest all the limitations of Claim 11.

Ito teaches that a decoder includes an instruction buffer (see Figure 3). Ito teaches that an instruction buffer stores instructions prior to decoding. Thus, at the very least, the instruction buffer of Ito is not an execution queue – the instructions stored in Ito's instruction buffers cannot be executed because they have not yet been decoded. One of ordinary skill in the art would understand that an execution queue stores decoded instructions. It is clear that the instruction buffer is not de-gated as only one instruction buffer is provided. De-gating the instruction buffer of Ito would terminate an executing program. Therefore, Ito fails to cure the deficiencies of Lavi.

Referring to Claim 21; Lavi teaches a CLIW reference instruction is discriminated from a regular instruction by an instruction decoder (see col. 10, lines 1-13). Lavi does not teach or suggest "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form and switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form" as claimed in Claim 21. Lavi teaches branch instructions for proceeding to a different location in a program (see col. 3, lines 30-34) – Lavi does not teach or suggest a branch instruction for switching between operation of the instruction decoder and the CLIW array – as shown above these operate in parallel. Indeed, the program of Lavi includes both regular instructions and reference instructions in order (see Figure 6) - no branch instruction is needed to switch between regular and reference instructions. The branch instruction operates to change a location without any

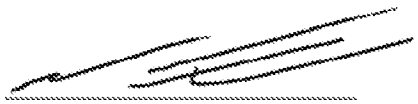
knowledge of regular and reference instructions. Further, the instructions of the instruction decoder and CLIW array are not of different forms – they are merely the result of different instructions of the same instruction set fetched from the program memory. The normal and reference instructions are fetched along the same pathway; Lavi has no need for a branch instruction back to the normal instructions because they are fetched along the same pathway as the reference instructions. Thus, Lavi fails to teach or suggest all the limitations of Claim 21.

Ito teaches that a decoder includes an instruction buffer (see Figure 3). Ito teaches a single instruction form being decoded by an instruction decoder. Thus, Ito fails to cure the deficiencies of Lavi.

For at least the forgoing reasons, the combined teachings of Lavi and Ito fail to teach or suggest all the limitations of Claims 1, 11, and 21. Therefore, there are clear errors in rejection of Claims 1, 11, and 21.

The application, including Claims 1-3, 5-13, and 15-21, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

By: 

Nathaniel T. Wallace
Reg. No. 48,909
Attorney for Applicant(s)

Mailing Address:
F. CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, New York 11797
TEL: (516) 692-8888
FAX: (516) 692-8889